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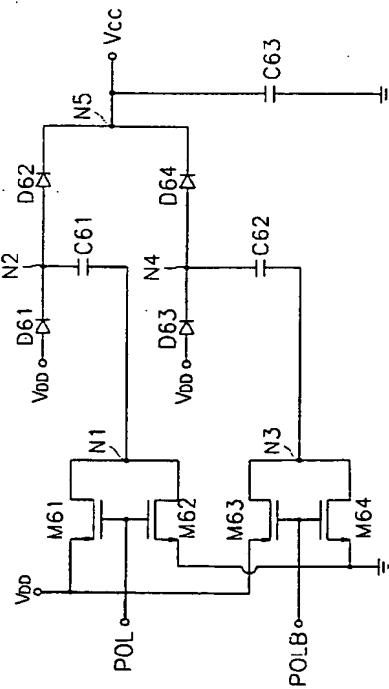
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(54) A DC-DC converter for a thin film transistor liquid crystal display

(57) A DC-DC converter for a TFT-LCD includes first and second switches (M61,M62) which are turned on/off in opposition according to a polar signal and third and fourth switches (M63,M64) which are turned on/off in opposition according to an inverse polar signal. First and second diodes (D61,D62) form electric paths in accordance with the first and the second switches, and third and fourth diodes (D63,D64) form electric paths in accordance with the third and fourth switches. A first ca-

pacitor (C61) is charged when the electric paths of the first and second diodes are provided and a second capacitor (C64) is charged when the electric paths of the third and fourth diodes are provided. A third capacitor (C63) is charged by the electric charges of the first and the second capacitors. Using this circuit, a DC-DC power converter can be constructed which uses very little power and therefore can be employed in a TFT-LCD of portable information processing equipment.

FIG. 6



Description

The present invention relates to a direct current-direct current (DC-DC) converter for a thin film transistor liquid crystal display (TFT-LCD), and more particularly, to a low power consumption DC-DC converter which can be used in displaying devices for portable information processing equipment.

A conventional DC-DC converter for a TFT-LCD will now be described. Fig. 1, is a graph illustrating a light-transmission ratio of a TFT-LCD. As illustrated in Fig. 1, TFT-LCD contrast increases with voltage because the light transmission ratio changes according to the applied voltage.

Fig. 2 is a detailed circuit diagram of a conventional gray voltage generating circuit. As shown in Fig. 2, a gray voltage is generated from the divided voltage of the resistors and the contrast is marked by applying one of the gray voltages to the liquid crystal capacitor.

Fig. 3 is a detailed circuit diagram of a conventional gray voltage generating circuit. As shown in Fig. 3, a conventional TFT-LCD includes a thin film transistor, a liquid crystal capacitor connected between a drain terminal and a common voltage Vcom of the TFT, plural gate lines, and switches connected to each source line and each gate line.

Operation of the conventional TFT-LCD described above will now be explained. First, one gray voltage of the plural gray voltages V1~V6 is selected with the switches S_m , S_{m+1} , S_{m+2} to S_{m+n} connected to the source line. Then, once a gate switch S_n connected to the gate line is turned on, the TFTs associated with this gate line are turned on by an applied voltage V_{on} to the gate terminal of the TFTs which are connected to an nth gate line. Once the TFTs of the nth line are turned on, the gray voltage on each source line is applied to the liquid crystal capacitors associated with the S_n gate line TFTs and the contrast is displayed on these liquid crystal capacitors. Thereafter, after one gray voltage of the gray voltages V1~V6 is selected with the switches S_m , S_{m+1} , S_{m+2} , to S_{m+n} connected to the respective source lines, the gate switch of the $n+1$ th line is turned on simultaneously as the gate switch of the nth line is turned off, and the power voltage V_{on} is then applied to the gate terminal of the TFTs connected to the $n+1$ th gate line and the TFTs associated with the $n+1$ th gate line are turned on. Once the TFTs of the $n+1$ th line are turned on, the gray voltage on each source line is applied to the associated liquid crystal capacitors via the $n+1$ th gate line TFTs and the contrast is displayed on the liquid crystal display.

If the above processing is repeated, a desired picture image can be formed wholly by such displayed contrast on the liquid crystal capacitors.

A typical TFT-LCD is driven by inverting by gate lines, once the nth gate line is selected, one of the gray voltages V1~V3 is loaded on the source line. Next, when the $n+1$ th gate line is selected, one of the gray voltages V4~V6 is loaded on the source line. Namely, in driving the line with inversion, as in Fig. 1 illustrating a relation between the voltage and the light-transmission ratio, once the curvilinear points of the relation between the voltage and the light-transmission ratio laid at the right side from Vcom are selected as the liquid crystal capacitor of one line, the curvilinear points of the relation between the voltage and the light-transmission ratio laid at the left side from Vcom are selected as the next liquid crystal capacitor of one line.

Since a signal which is used as the basis of selecting a polarity of the liquid crystal capacitor, is one of polar signal POL or inverse polar signal POLB as illustrated in Fig. 4, the switches S_m , S_{m+1} , S_{m+2} select one of the gray voltages V1~V3 or V4~V6 on the basis of the signals POL, POLB. For instance, one voltage of the gray voltages V1~V3 is selected when a polar signal POL is at a Vdd level, one voltage of the gray voltages V4~V6 is selected when the polar signal POL is at a GND level.

In the gray voltage generating circuit, as illustrated in Fig. 2, a power voltage V_{cc} is an output power source of the DC-DC converter which is at a voltage level above 8V. The DC-DC converter converts from a Vdd power source of 5V level to a direct current power voltage V_{cc} of above 8V.

Fig. 5 is a detailed circuit diagram illustrating a conventional DC-DC converter. As shown in Fig. 5, a conventional DC-DC converter for a TFT-LCD includes a pulse width modulation integrated circuit PWMIC 51 having a power terminal connected to the power source Vdd, a coil L51 having one terminal connected to the power source Vdd, a transistor Q51 having a collector terminal connected to the other terminal of the coil L51, a base terminal connected to an output terminal of the PWMIC 51 and a grounded emitter terminal, a diode D51 having an anode terminal connected to the collector terminal of the transistor Q51 and a capacitor C51 connected between a cathode terminal and a ground of the diode D51.

Operation of this conventional DC-DC converter for a TFT-LCD will now be described. A PWMIC 51 generates a rectangular pulse and controls a duty ratio, so that a constant DC voltage will be output. If an output DC voltage is above a predetermined value, the duty ratio is reduced, thereby lower the output DC voltage, and vice versa.

The transistor Q51 is turned on when the rectangular pulse outputted from the output terminal of the PWMIC 51 is at a high level and the amount of power flowing through the coil L51 is increasing in proportion to the time.

The amount of the power I_L is calculated according to the following equation:

$$I_L = \frac{Vdd}{V} T \quad (1)$$

In equation (1), T denotes a turn-on time of the transistor Q51.

5 Next, the transistor Q51 is turned off when the rectangular pulse outputted from the output terminal of the PWMIC 51 is at a low level, thus causing the power flowing through coil L51 to be cut off, and causing a high voltage to turn on the diode D51, so that the power accumulated as a magnetic field on the coil L51 may flow through the diode D51 and charge the capacitor C51. The charged voltage Vcc is used for the power voltage to generate a gray voltage.

10 However, the prior DC-DC converter for a TFT-LCD consumes too much power. Although the actual power consumed by the DC-DC converter is only 3mA, the power needed for the electronic circuit, PWMIC, internal resistance of the coil, of the DC-DC converter is more than 20 mA.

The power conversion efficiency may be expressed according to equation 2:

$$15 \frac{\text{output power}}{\text{input power}} \times 100\% = \frac{Vcc \times 3mA \times 100\%}{Vdd \times 20 \text{ mA} + Vcc \times 3mA} \quad (2)$$

In equation (2), if Vdd=5V, Vcc=8V, the power conversion efficiency of a conventional DC-DC converter is only 20%, which is too wasteful to realistically be applied to a portable information processing equipment display.

20 An object of the present invention is to solve the problems involved in conventional apparatuses, and to provide a DC-DC converter for a TFT-LCD to be used in portable information processing equipment which itself requires very little power.

25 To achieve this object and others, the present invention includes first and second switches which are turned on or off in opposition according to a polar signal. First and second diodes form electric paths by being turned on when the first and second switches are turned on to thereby charge a first capacitor. Third and fourth switches are turned on/off in opposition according to an inverse polar signal. Third and fourth diodes form electric paths when the third and fourth switches are turned on to thereby charge a second capacitor. A third capacitor is charged by the electric charges of the first and the second capacitors.

30 Preferably, the polar signal and the inverse polar signal have opposite phases. PMOS or NMOS type transistors can form the four switches and first and second diodes, and third and fourth diodes may be serially connected in positive direction. Plural diodes may be connected to form any one diode.

The preferred embodiments of the present invention will now be described more specifically with reference to the attached drawings, wherein:

- 35 Fig. 1 is a graph illustrating a liquid crystal light-transmission ratio;
 Fig. 2 is a detailed circuit diagram of a conventional gray voltage generating circuit;
 Fig. 3 is a detailed circuit diagram of a conventional TFT-LCD;
 Fig. 4 is a wave form for an inverse driving of a typical TFT-LCD;
 Fig. 5 is a detailed circuit diagram of a conventional TFT-LCD;
 Fig. 6 is a detailed circuit diagram of a DC-DC converter for TFT-LCD according to a preferred embodiment of the
 40 present invention; and
 Fig. 7 is a wave form illustrating each sectional operation of a DC-DC converter for a TFT-LCD according to a preferred embodiment of this invention.

A preferred embodiment will now be described with particular reference to Figs. 6 and 7.

45 As shown in Fig. 6, a DC-DC converter for a TFT-LCD according to a preferred embodiment of this invention includes transistors M61, M62 having their source terminals connected to a power signal line Vdd and a ground signal line GND, respectively, and their gate terminals connected in common to a polar signal line POL. The converter also includes transistors M63, M64 having their source terminals connected to the power signal line Vdd and the grounded signal line GND, respectively, and their gate terminal jointly connected to a inverse polar signal line POLB.

50 Diodes D61 and D63 are provided, the anodes of which are connected to power signal line Vdd. Diodes D62 and D64 have their anode terminals connected to the cathode terminals of diodes D61 and D63, respectively. The cathode terminals of the diodes D62 and D64 are connected together, and a capacitor is connected between the cathode terminals of the diodes D62, D64 and ground.

55 In the preferred embodiment of the invention, the diodes D61, D62, D63, and D64 are used in pairs with each signal POL or POLB, however plural diodes can be used instead of only two diodes.

Operation of the TFT-LCD according to the preferred embodiment of the invention is described below.

As illustrated in Fig. 7, when the signal POL has a ground potential, the power signal Vdd is applied to a Node N1 by turning on the PMOS type transistor M61. When the POL is at a power level, the ground level signal is applied to

a node N1 by turning on the NMOS type transistor M62. Accordingly, a pulse wave form signal is generated in the node N1 according to the POL signal as illustrated in Fig. 7.

When the node N1 is at a ground level, the electrons applied through the diode D61 are charged to the capacitor C61. The amount of charge accumulated by the capacitor C61 is calculated according to equation 3 below:

5

$$Q_{61} = C_{61} \times (V_{dd} - V_d) \quad (3)$$

in which V_d denotes the voltage drop across the diode D61.

When the node N1 is at a power level V_{dd} , the potential of the node N2 is $(V_{dd} + Q_{61}/C_{61})$, which may be combined with equation 3 to get $(2V_{dd} - V_d)$. In this case the diode D61 is turned off from the applied reverse-bias, and the electrons at node N2 are transferred to the capacitor C63 by turning on the diode D62.

The amount of the electrons Q_{63} charged to the capacitor C63 flows though the diode D62 until the diode D62 is turned off, and is calculated according to equation 4 below:

15

$$Q_{63} = C_{63} \times 2 \times (V_{dd} - V_d) \quad (4)$$

Since the voltage V_{cc} of the node N5 is (Q_{63}/C_{63}) , the voltage V_{cc} is $2(V_{dd} - V_d)$.

As illustrated in Fig. 7, when the inverse polar signal POLB is at a ground level, the PMOS type transistor M63 is turned on and a power signal V_{dd} is applied to the node N3. When the inverse polar signal POLB is at a power level V_{dd} , the NMOS type transistor M64 is turned on and the ground level signal is applied to the node N3. Accordingly, a pulse wave form signal as in Fig. 7 is generated to the node N3 in accordance to the inverse polar signal POLB.

When the node is at a ground level, the electrons applied through the diode D63 are charged to the capacitor C62, the amount of electron Q_{62} charged to the capacitor C62 is calculated as the equation 5 below:

$$Q_{62} = C_{62} \times (V_{dd} - V_d) \quad (5)$$

30 where V_d is the voltage drop across the diode D63.

When the node N3 is at a power level V_{dd} , a potential of the node N4 is $(V_{dd} + Q_{62}/C_{62})$ and results in $(2V_{dd} - V_d)$ with the equation 5. In this case the diode D63 is turned off from the applied reverse-bias, and the electron of the node N4 is charged to the capacitor C63 by the turn on of the diode D64.

35 The charge Q_{63} applied to the capacitor C63 flows though the diode D64 until the diode D64 is turned off, and is calculated as the equation 6 below.

$$Q_{63} = C_{63} \times 2 \times (V_{dd} - V_d) \quad (6)$$

40 Since the voltage V_{cc} of the node N5 is (Q_{63}/C_{63}) the voltage V_{cc} is equal to $2(V_{dd} - V_d)$.

The polar signal POL and the inverse polar signal POLB are of opposite phase. Therefore, generalizing the whole operation, a constant direct current voltage V_{cc} equal to $2(V_{dd} - V_d)$, is outputted to the node N5 as illustrated in Fig. 7. Accordingly, the small power consuming DC-DC converter can be provided by supplying a stabilized direct current voltage V_{cc} using MOS transistors M61 to M64 and diodes D61 to D64 which consume low amounts of power. If a number of the diodes D61 to D64 is controlled, the value of the direct current voltage V_{cc} can be randomly set.

45 The preferred embodiment of the invention provides a DC-DC converter for a TFT-LCD which may be used in portable information processing equipment because the DC-DC converter consumes very little power.

It is understood that various other modifications will be apparent to and can be readily made by those skilled in the art without departing from the scope and spirit of this invention. Accordingly, it is not intended that the scope of the 50 claims appended hereto be limited to the description as set forth herein, but rather that the claims be construed as encompassing all the features of patentable novelty that reside in the present invention, including all features that would be treated as equivalents thereof by those skilled in the art which this invention pertains.

55 Claims

1. A DC-DC converter for a TFT-LCD, comprising:

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a first switch and a second switch which are turned on and off in opposition according to a polar signal; a first diode and a second diode which form electric paths by being turned on when the first and the second switches are turned on;

- 5 a first capacitor which charges when the electric paths of the first and the second diodes are formed; a third diode and a fourth diode which form electric paths by being turned on when the third and the forth switches are turned on; a second capacitor which charges when the electric paths of the third and the fourth diodes are formed; and a third capacitor which is charged by the electric charges of the first and the second capacitors.

10 2. A DC-DC converter for a TFT-LCD as claimed in Claim 1, wherein said polar signal and the inverse polar signal have opposite phases.

15 3. A DC-DC converter for a TFT-LCD as claimed in Claim 1 or Claim 2, wherein said first switch and second switch, said third switch and said fourth switch each use a PMOS or NMOS type transistor.

4. A DC-DC converter for a TFT-LCD as claimed in any of Claims 1 to 3, wherein said first diode and second diode, and said third diode and said fourth diode are respectively serially connected in a positive direction.

20 5. A DC-DC converter for a TFT-LCD, comprising:

25 a switch circuit which inputs a pulsed polar signal and an inverse polar pulse signal and outputs a first pulsed voltage to a first node and a second pulsed voltage to a second node; a charge circuit connected between said first and second nodes and an output node, said charge circuit further connected to a power source having a power source voltage such that third and forth nodes within said charging circuit are intermittently raised by a capacitor to a charging voltage level which exceeds said power source voltage; said third and fourth nodes each connected through a diode to said output node; and a smoothing capacitor connected to said output node.

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FIG.1

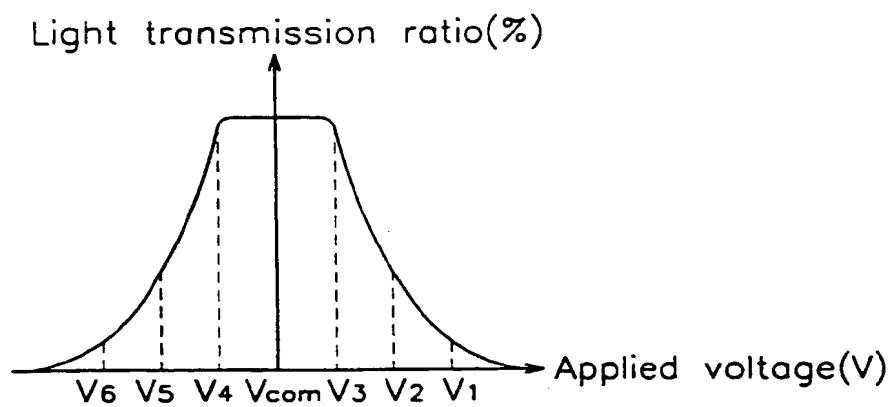


FIG.2 (Prior Art)

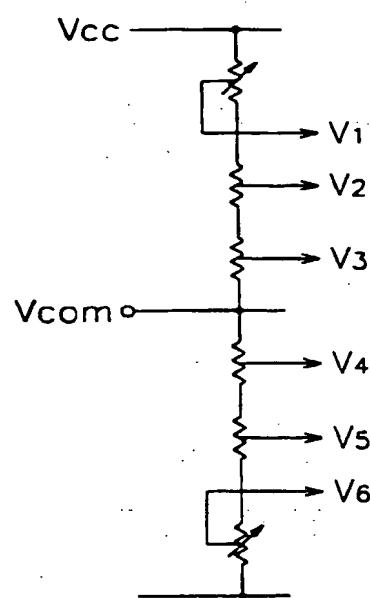


FIG. 3 (Prior Art)

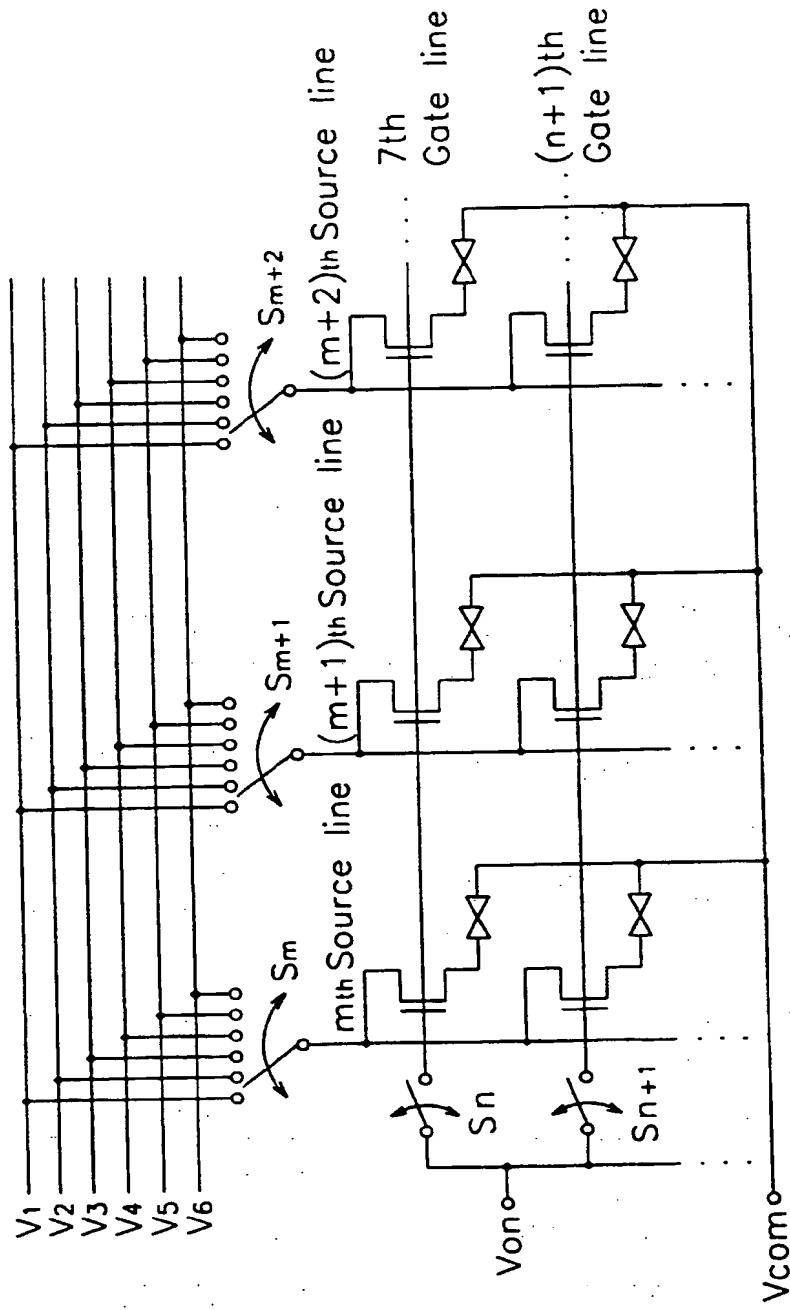


FIG.4(Prior Art)

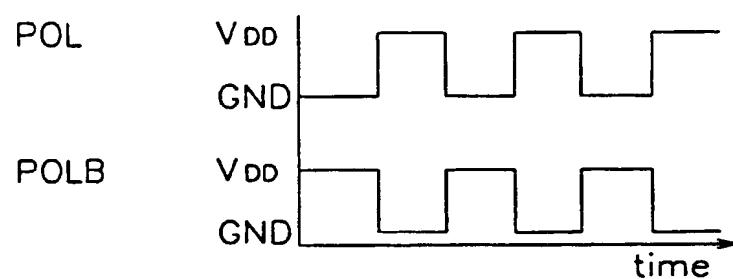


FIG.5(Prior Art)

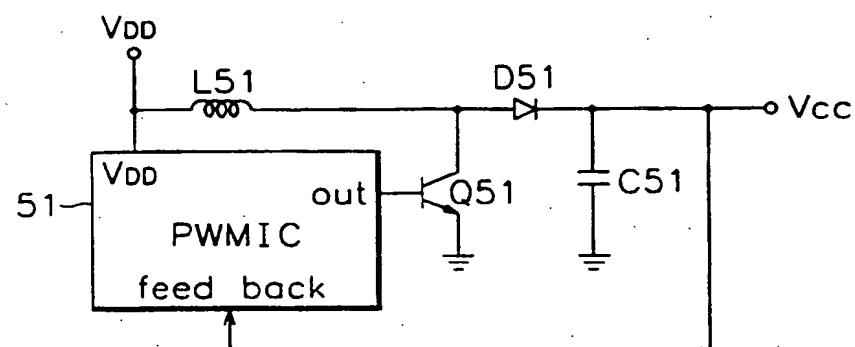


FIG.6

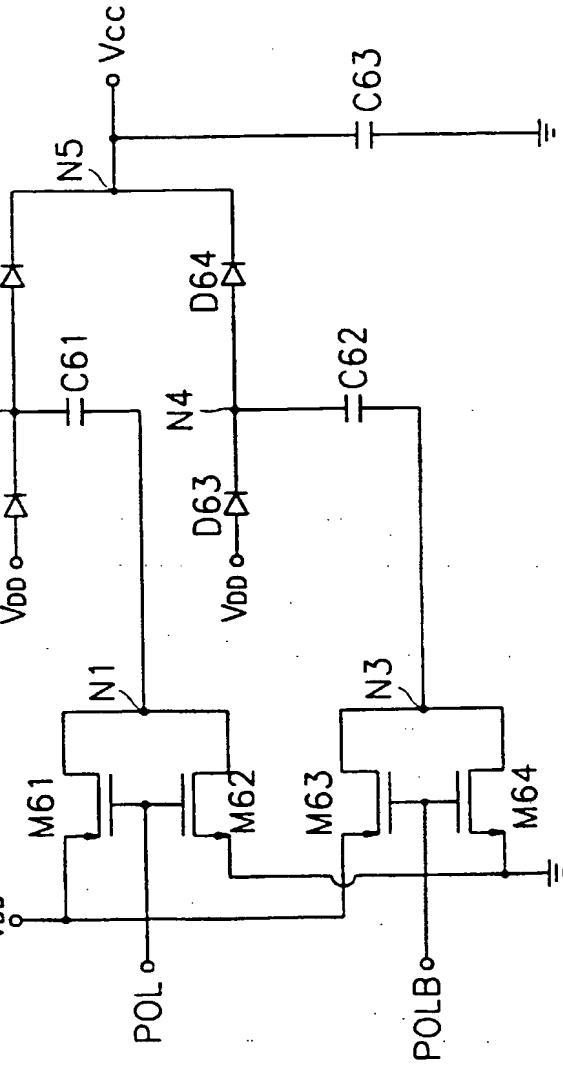
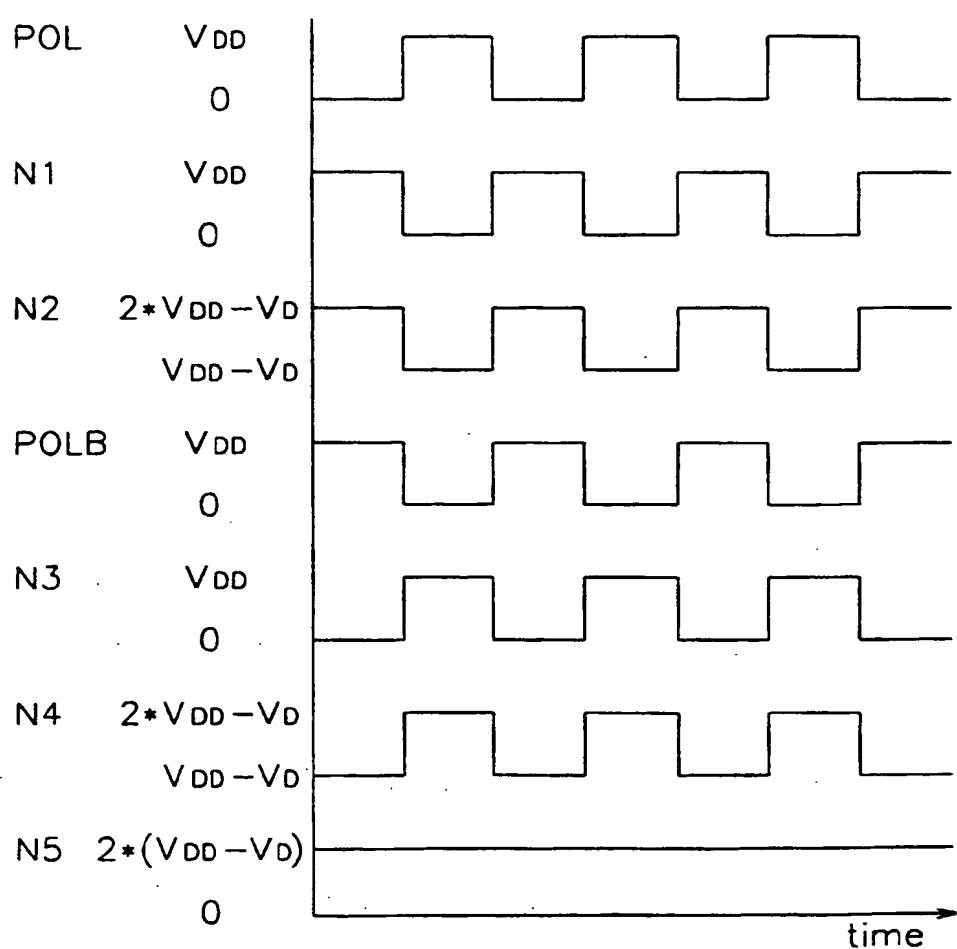


FIG. 7





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EUROPEAN SEARCH REPORT

Application Number
EP 96 30 2619

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	US 5 036 229 A (TRAN DUNG Q) 30 July 1991 * figures 7,11 *	1-5	G09G3/36 H02M3/07
A	US 3 818 484 A (NAKAMURA T ET AL) 18 June 1974 * figure 3 *	1,3,5	
A	GB 2 078 021 A (HITACHI LTD) 23 December 1981 * abstract; figure 7 *	1,5	
<p>)</p> <p>The present search report has been drawn up for all claims</p>			
<p>Place of search THE HAGUE</p>		<p>Date of completion of the search 26 November 1996</p>	Examiner Verhoof, P
<p>CATEGORY OF CITED DOCUMENTS</p> <p>X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document</p> <p>T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application I : document cited for other reasons & : member of the same patent family, corresponding document</p>			